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(57) Abstract			
<p>This invention relates to methods for in-line sampling of a semiconductor wafer for monitoring purposes while preserving at least significant integrity of the parent wafer. More specifically, the invention employs focused ion beam technology and electrostatic probes or a mechanical assembly, e.g., tweezers, to cut and remove a segment of a semiconductor wafer, while in process, for analysis, and to fill the void by deposition of a dielectric material on the wafer, thus preserving essential integrity of the wafer. The removed segment allows extensive analysis of the wafer, such as defect analysis, without sacrificing the entire wafer in the process. The invention can include the further step of filling the cavity that has been created in the wafer as a result of removing the segment. The deposition of the dielectric material closes the opening and restores the wafer surface to its original or other desired topography. In addition, it limits the level of contamination of the wafer by the ions of the FIB employed to cut out the removed segment.</p>			
<pre>graph TD A[IMAGING SILICON WAFER BY AN FIB TO SELECT LOCATION FOR REMOVAL] --> B[ETCHING THE WAFER BY AN FIB TO CUT A SEGMENT AT SELECTED LOCATION] B --> C[REMOVING THE CUT SEGMENT BY AN ELECTROSTATIC PROBE] C --> D[PLACING THE REMOVED SEGMENT ON A HOLDER] C --> E[DEPOSITING SILICON DIOXIDE ON THE WAFER TO FILL VOID CREATED BY REMOVAL] D --> F[ANALYZING THE REMOVED SEGMENT] F --> G[] E --> G G --> H[] H --> I[] I --> J[] J --> K[] K --> L[] L --> M[] M --> N[] N --> O[] O --> P[] O --> Q[] O --> R[] O --> S[] O --> T[] O --> U[] O --> V[] O --> W[] O --> X[] O --> Y[] O --> Z[] O --> AA[] O --> AB[] O --> AC[] O --> AD[] O --> AE[] O --> AF[] O --> AG[] O --> AH[] O --> AI[] O --> AJ[] O --> AK[] O --> AL[] O --> AM[] O --> AN[] O --> AO[] O --> AP[] O --> AQ[] O --> AR[] O --> AS[] O --> AT[] O --> AU[] O --> AV[] O --> AW[] O --> AX[] O --> AY[] O --> AZ[] O --> BA[] O --> BB[] O --> BC[] O --> BD[] O --> BE[] O --> BF[] O --> BG[] O --> BH[] O --> BI[] O --> BJ[] O --> BK[] O --> BL[] O --> BM[] O --> BN[] O --> BO[] O --> BP[] O --> BQ[] O --> BR[] O --> BS[] O --> BT[] O --> BU[] O --> BV[] O --> BW[] O --> BX[] O --> BY[] O --> BZ[] O --> CA[] O --> CB[] O --> CC[] O --> CD[] O --> CE[] O --> CF[] O --> CG[] O --> CH[] O --> CI[] O --> CJ[] O --> CK[] O --> CL[] O --> CM[] O --> CN[] O --> CO[] O --> CP[] O --> CQ[] O --> CR[] O --> CS[] O --> CT[] O --> CU[] O --> CV[] O --> CW[] O --> CX[] O --> CY[] O --> CZ[] O --> DA[] O --> DB[] O --> DC[] O --> DD[] O --> DE[] O --> DF[] O --> DG[] O --> DH[] O --> DI[] O --> DJ[] O --> DK[] O --> DL[] O --> DM[] O --> DN[] O --> DO[] O --> DP[] O --> DQ[] O --> DR[] O --> DS[] O --> DT[] O --> DU[] O --> DV[] O --> DW[] O --> DX[] O --> DY[] O --> DZ[] O --> EA[] O --> EB[] O --> EC[] O --> ED[] O --> EE[] O --> EF[] O --> EG[] O --> EH[] O --> EI[] O --> EJ[] O --> EK[] O --> EL[] O --> EM[] O --> EN[] O --> EO[] O --> EP[] O --> EQ[] O --> ER[] O --> ES[] O --> ET[] O --> EU[] O --> EV[] O --> EW[] O --> EX[] O --> EY[] O --> EZ[] O --> FA[] O --> FB[] O --> FC[] O --> FD[] O --> FE[] O --> FF[] O --> FG[] O --> FH[] O --> FI[] O --> FJ[] O --> FK[] O --> FL[] O --> FM[] O --> FN[] O --> FO[] O --> FP[] O --> FQ[] O --> FR[] O --> FS[] O --> FT[] O --> FU[] O --> FV[] O --> FW[] O --> FX[] O --> FY[] O --> FZ[] O --> GA[] O --> GB[] O --> GC[] O --> GD[] O --> GE[] O --> GF[] O --> GG[] O --> GH[] O --> GI[] O --> GJ[] O --> GK[] O --> GL[] O --> GM[] O --> GN[] O --> GO[] O --> GP[] O --> GQ[] O --> GR[] O --> GS[] O --> GT[] O --> GU[] O --> GV[] O --> GW[] O --> GX[] O --> GY[] O --> GZ[] O --> HA[] O --> HB[] O --> HC[] O --> HD[] O --> HE[] O --> HF[] O --> HG[] O --> HH[] O --> HI[] O --> HJ[] O --> HK[] O --> HL[] O --> HM[] O --> HN[] O --> HO[] O --> HP[] O --> HQ[] O --> HR[] O --> HS[] O --> HT[] O --> HU[] O --> HV[] O --> HW[] O --> HX[] O --> HY[] O --> HZ[] O --> IA[] O --> IB[] O --> IC[] O --> ID[] O --> IE[] O --> IF[] O --> IG[] O --> IH[] O --> II[] O --> IJ[] O --> IK[] O --> IL[] O --> IM[] O --> IN[] O --> IO[] O --> IP[] O --> IQ[] O --> IR[] O --> IS[] O --> IT[] O --> IU[] O --> IV[] O --> IW[] O --> IX[] O --> IY[] O --> IZ[] O --> JA[] O --> JB[] O --> JC[] O --> JD[] O --> JE[] O --> JF[] O --> JG[] O --> JH[] O --> JI[] O --> JJ[] O --> JK[] O --> JL[] O --> JM[] O --> JN[] O --> JO[] O --> JP[] O --> JQ[] O --> JR[] O --> JS[] O --> JT[] O --> JU[] O --> JV[] O --> JW[] O --> JX[] O --> JY[] O --> JZ[] O --> KA[] O --> KB[] O --> KC[] O --> KD[] O --> KE[] O --> KF[] O --> KG[] O --> KH[] O --> KI[] O --> KJ[] O --> KL[] O --> KM[] O --> KN[] O --> KO[] O --> KP[] O --> KQ[] O --> KR[] O --> KS[] O --> KT[] O --> KU[] O --> KV[] O --> KW[] O --> KX[] O --> KY[] O --> KZ[] O --> LA[] O --> LB[] O --> LC[] O --> LD[] O --> LE[] O --> LF[] O --> LG[] O --> LH[] O --> LI[] O --> LJ[] O --> LK[] O --> LL[] O --> LM[] O --> LN[] O --> LO[] O --> LP[] O --> LQ[] O --> LR[] O --> LS[] O --> LT[] O --> LU[] O --> LV[] O --> LW[] O --> LX[] O --> LY[] O --> LZ[] O --> MA[] O --> MB[] O --> MC[] O --> MD[] O --> ME[] O --> MF[] O --> MG[] O --> MH[] O --> MI[] O --> MJ[] O --> MK[] O --> ML[] O --> MN[] O --> MO[] O --> MP[] O --> MQ[] O --> MR[] O --> MS[] O --> MT[] O --> MU[] O --> MV[] O --> MW[] O --> MX[] O --> MY[] O --> MZ[] O --> NA[] O --> NB[] O --> NC[] O --> ND[] O --> NE[] O --> NF[] O --> NG[] O --> NH[] O --> NI[] O --> NJ[] O --> NK[] O --> NL[] O --> NM[] O --> NN[] O --> NO[] O --> NP[] O --> NQ[] O --> NR[] O --> NS[] O --> NT[] O --> NU[] O --> NV[] O --> NW[] O --> NX[] O --> NY[] O --> NZ[] O --> OA[] O --> OB[] O --> OC[] O --> OD[] O --> OE[] O --> OF[] O --> OG[] O --> OH[] O --> OI[] O --> OJ[] O --> OK[] O --> OL[] O --> OM[] O --> ON[] O --> OO[] O --> OP[] O --> OQ[] O --> OR[] O --> OS[] O --> OT[] O --> OU[] O --> OV[] O --> OW[] O --> OX[] O --> OY[] O --> OZ[] O --> PA[] O --> PB[] O --> PC[] O --> PD[] O --> PE[] O --> PF[] O --> PG[] O --> PH[] O --> PI[] O --> PJ[] O --> PK[] O --> PL[] O --> PM[] O --> PN[] O --> PO[] O --> PP[] O --> PQ[] O --> PR[] O --> PS[] O --> PT[] O --> PU[] O --> PV[] O --> PW[] O --> PX[] O --> PY[] O --> PZ[] O --> QA[] O --> QB[] O --> QC[] O --> QD[] O --> QE[] O --> QF[] O --> QG[] O --> QH[] O --> QI[] O --> QJ[] O --> QK[] O --> QL[] O --> QM[] O --> QN[] O --> QO[] O --> QP[] O --> QQ[] O --> QR[] O --> QS[] O --> QT[] O --> QU[] O --> QV[] O --> QW[] O --> QX[] O --> QY[] O --> QZ[] O --> RA[] O --> RB[] O --> RC[] O --> RD[] O --> RE[] O --> RF[] O --> RG[] O --> RH[] O --> RI[] O --> RJ[] O --> RK[] O --> RL[] O --> RM[] O --> RN[] O --> RO[] O --> RP[] O --> RQ[] O --> RR[] O --> RS[] O --> RT[] O --> RU[] O --> RV[] O --> RW[] O --> RX[] O --> RY[] O --> RZ[] O --> SA[] O --> SB[] O --> SC[] O --> SD[] O --> SE[] O --> SF[] O --> SG[] O --> SH[] O --> SI[] O --> SJ[] O --> SK[] O --> SL[] O --> SM[] O --> SN[] O --> SO[] O --> SP[] O --> SQ[] O --> SR[] O --> SS[] O --> ST[] O --> SU[] O --> SV[] O --> SW[] O --> SX[] O --> SY[] O --> SZ[] O --> TA[] O --> TB[] O --> TC[] O --> TD[] O --> TE[] O --> TF[] O --> TG[] O --> TH[] O --> TI[] O --> TJ[] O --> TK[] O --> TL[] O --> TM[] O --> TN[] O --> TO[] O --> TP[] O --> TQ[] O --> TR[] O --> TS[] O --> TT[] O --> TU[] O --> TV[] O --> TW[] O --> TX[] O --> TY[] O --> TZ[] O --> UA[] O --> UB[] O --> UC[] O --> UD[] O --> UE[] O --> UF[] O --> UG[] O --> UH[] O --> UI[] O --> UJ[] O --> UK[] O --> UL[] O --> UM[] O --> UN[] O --> UO[] O --> UP[] O --> UQ[] O --> UR[] O --> US[] O --> UT[] O --> UY[] O --> UZ[] O --> VA[] O --> VB[] O --> VC[] O --> VD[] O --> VE[] O --> VF[] O --> VG[] O --> VH[] O --> VI[] O --> VJ[] O --> VK[] O --> VL[] O --> VM[] O --> VN[] O --> VO[] O --> VP[] O --> VQ[] O --> VR[] O --> VS[] O --> VT[] O --> VU[] O --> VV[] O --> VW[] O --> VX[] O --> VY[] O --> VZ[] O --> WA[] O --> WB[] O --> WC[] O --> WD[] O --> WE[] O --> WF[] O --> WG[] O --> WH[] O --> WI[] O --> WJ[] O --> WK[] O --> WL[] O --> WM[] O --> WN[] O --> WO[] O --> WP[] O --> WQ[] O --> WR[] O --> WS[] O --> WT[] O --> WY[] O --> WZ[] O --> XA[] O --> XB[] O --> XC[] O --> XD[] O --> XE[] O --> XF[] O --> XG[] O --> XH[] O --> XI[] O --> XJ[] O --> XK[] O --> XL[] O --> XM[] O --> XN[] O --> XO[] O --> XP[] O --> XQ[] O --> XR[] O --> XS[] O --> XT[] O --> XU[] O --> XV[] O --> XW[] O --> XX[] O --> XY[] O --> XZ[] O --> YA[] O --> YB[] O --> YC[] O --> YD[] O --> YE[] O --> YF[] O --> YG[] O --> YH[] O --> YI[] O --> YJ[] O --> YK[] O --> YL[] O --> YM[] O --> YN[] O --> YO[] O --> YP[] O --> YQ[] O --> YR[] O --> YS[] O --> YT[] O --> YU[] O --> YV[] O --> YW[] O --> YX[] O --> YY[] O --> YZ[] O --> ZA[] O --> ZB[] O --> ZC[] O --> ZD[] O --> ZE[] O --> ZF[] O --> ZG[] O --> ZH[] O --> ZI[] O --> ZJ[] O --> ZK[] O --> ZL[] O --> ZM[] O --> ZN[] O --> ZO[] O --> ZP[] O --> ZQ[] O --> ZR[] O --> ZS[] O --> ZT[] O --> ZU[] O --> ZV[] O --> ZW[] O --> ZX[] O --> ZY[] O --> ZZ[]</pre>			

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IN-LINE FIB PROCESS MONITORING WITH WAFER PRESERVATION

Background

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This invention relates to methods for sampling a semiconductor wafer while preserving essential integrity of the wafer. More specifically, the invention relates to methods for in-line process monitoring of a semiconductor wafer without sacrificing the entire wafer in the process.

10

The process monitoring of fabricated semiconductor wafers is traditionally accomplished by removing the wafer from the manufacturing process for analysis. Such methods traditionally render the entire wafer unusable for further processing. Thus, the wafer used for analysis is discarded.

15

Although the wafer may be imaged by a focused ion beam ("FIB"), while still in process, to search for defects, the imaging capability of an FIB, even with integration of a scanning electron microscope ("SEM"), is not as good as that of a single column SEM. The imaging capability of an FIB is further limited by inaccessibility for imaging of side surfaces of structural blocks on the wafer.

20

Furthermore, choices of chemicals for decoration of the sample are limited due to incompatibility of many chemicals used for decoration with the materials inside an FIB chamber. In addition, in the case of an FIB that uses Gallium ions, extensive contamination of the silicon wafer can occur, rendering the wafer not usable after exposure to the Gallium beam.

25

Thus, wafers used for conventional process monitoring are typically removed from the FIB system, a portion of the wafer is analyzed, and then the wafer is discarded. This discarding of an entire wafer, including valuable intact circuit devices, can result in a significant financial loss. As a wafer enters the advanced stages of processing, the financial loss associated with discarding a wafer increases significantly. It is therefore desirable to develop methods which allow in-line process monitoring of semiconductor wafers without loss of the entire wafer.

30

U.S. Patent No. 5,270,552 issued to Ohnishi et al (hereinafter Ohnishi), and incorporated herein by reference, relates to monitoring of FIB processing of wafers. The present invention provides improvements over what is taught in Ohnishi. The improvements of the present invention include avoiding damage to the wafer and monitoring the FIB processing of wafers in a quick and effective manner.

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Accordingly it is an object of this invention to provide a method for in-line sampling of a semiconductor wafer while preserving essential integrity of the parent wafer.

5 The invention is next described in connection with an illustrated embodiment. It will, however, be obvious to those skilled in the art that various modifications can be made to the embodiment without departing from the spirit or scope of this invention.

Summary of the Invention

10 This invention relates to methods for in-line sampling of a semiconductor wafer for monitoring purposes while preserving at least significant integrity of the parent wafer. More specifically, the invention employs focused ion beam technology and electrostatic probes or a mechanical assembly, e.g., tweezers, to cut and remove a segment of a semiconductor wafer, while in process, for analysis, and to fill the void by
15 deposition of a dielectric material on the wafer, thus preserving essential integrity of the wafer. The removed segment allows extensive analysis of the wafer, such as defect analysis, without sacrificing the entire wafer in the process.

The invention typically is practiced on a wafer of dielectric material, such as silicon, that is treated with integrated circuit fabricating steps such as selective impurity
20 doping, passivation, chemical etching, material deposition, and the like. In one embodiment of the invention, the wafer is imaged by a focused ion beam to select a location to be analyzed. The location can be selected for example by seemingly faulty appearance, faulty in situ testing, or otherwise. After selecting the location that includes circuitry of interest or other wafer positions, a focused ion beam, capable of etching the
25 semiconductor wafer, is directed to that location on the wafer to cut from the wafer a segment of selected size, including depth, at that location. In one embodiment of the invention, three straight milling cuts are performed. The cuts in this example penetrate the wafer to a depth of approximately 30 microns, at three sides of the segment to be removed. A further cut, is performed at an angle of approximately 45-60 degrees to the
30 normal in such a way that a pyramidal polyhedron is milled with one corner well inside the bulk of the wafer. In such a case, the cross section of the cut segment viewed from the top is a square. In another embodiment, the segment is cut by making three milling cuts such that the cross sections of the cut segment viewed from the top and from each side are triangular.

35 An electrostatic probe, brought to the proximity of the top side of the cut segment, removes the segment from the bulk of the wafer. Alternatively, mechanical tweezers can remove the segment. The removed segment is then available for analysis

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without further deteriorating or otherwise affecting the wafer from which it was cut. Once on a sample holder, extensive analysis of the removed segment is feasible. For example, the removed segment can be placed in a high resolution scanning electron microscope ("SEM"), it can be chemically decorated, or it can undergo a variety of material analyses.

The invention can include the further step of filling the cavity that has been created in the wafer as a result of removing the segment. The deposition of the dielectric material closes the opening and restores the wafer surface to its original or other desired topography. In addition, it limits the level of contamination of the wafer by the ions of the FIB employed to cut out the removed segment. In one embodiment of the invention, the semiconductor wafer is silicon, and Gallium ions are used for etching it to remove the segment. Because Gallium ions can diffuse readily into silicon, the deposition of the dielectric material after removal of the segment encapsulates any contaminated silicon, thus reducing the risk of large area contamination.

Thus, the invention allows in-line process monitoring and defect analysis of a semiconductor wafer while preserving the integrity of the parent wafer.

Brief Description of the Drawings

FIGURE 1 is a flow chart delineating steps according to the invention for in-line sampling of a semiconductor wafer.

FIGURE 2 depicts a semiconductor wafer from which a segment has been cut according to the invention.

FIGURE 3(a) to FIGURE 3(e) schematically illustrate processes of separation in an embodiment of the separation method according to the present invention.

FIGURE 4(a) and FIGURE 4(b) schematically illustrate an example of a separation process for separating a specimen which can be processed in a transmission electron microscope (TEM).

FIGURE 5(a) and FIGURE 5(b) schematically illustrate another example of a separation process for separating a specimen which can be processed in a transmission electron microscope (TEM).

Description of illustrated Embodiment

FIGURE 1 shows a flow chart depicting various steps in an illustrated embodiment of the present invention. The first step of the process consists of imaging the silicon wafer by focusing a beam of Gallium ions on the surface of the wafer and detecting the emitted secondary ions. The imaging of the wafer allows selection of the location where it is desirable to remove a segment for analysis.

Further reference to FIGURE 1 also shows that after selection of the appropriate location for removal of a segment, an FIB, capable of etching a silicon wafer, is used to cut away a segment of the wafer. In one practice of the invention, illustrated in FIGURE 2, three straight milling cuts are performed to a depth of approximately 30 microns, and then a final cut is performed at an angle of 45-60 degrees to the normal to the wafer in such a way that a pyramidal polyhedron solid is milled with one corner well inside the bulk silicon.

FIGURE 1 also shows that an electrostatic probe is brought to the proximity of the cut segment in order to remove the segment from the bulk silicon wafer. The FIB system then bonds the probe to the cut segment. Subsequently, a user can manipulate the probe to place the removed segment onto a segment or sample holder. The cut segment can then be analyzed by a variety of known techniques, such as SEM.

With further reference to FIGURE 1, after the segment is removed from the wafer, an FIB is used to deposit silicon dioxide on the wafer at the location where the segment was removed. The deposition is accomplished by introducing chemicals, such as those in the siloxane family and typically in a vapor state, to the surface of the wafer in the presence of an FIB of Gallium ions incident on the wafer at the location of the removed segment. The beam of Gallium ions interacts with the chemicals to deposit silicon dioxide onto the wafer. The deposition at least coats or covers the surface where the segment was cut from the wafer. It typically fills the cavity created by the removal of the cut segment, and can restore the surface of the wafer to its original topography. Because Gallium ions are contaminants in silicon, coating the cuts in the wafer with such a dielectric as silicon dioxide reduces the risk of large area contamination by encapsulating any contaminated silicon.

FIGURE 1 further shows that the steps of imaging, etching the wafer to cut a segment of the wafer, and depositing dielectric material on the wafer, are accomplished in a high vacuum chamber. The step of removing the cut segment can be either performed under high vacuum, or can be accomplished externally by removing the wafer from the vacuum chamber.

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FIGURE 2 shows the geometry of one embodiment of a sample cut from a wafer according to one method of the present invention.

Next, with reference to FIGS. 3 (a) - 3 (e), the processing on the specimen 12 by means of an FIB apparatus will be described. FIG. 3 (a) to FIG. 3 (e) show an embodiment of the present invention, illustrating steps (a) through (e) for separating from the specimen 12, a part of the specimen 12 including a portion to be analyzed. In this embodiment, the specimen 12 is silicon substrate, and the separated part of the specimen 12 is hereinafter referred to as "a separated specimen". The process of separation will be described along the steps (a) through (e) successively.

10 (a) In FIG. 3 (a), the attitude of the specimen 12 is maintained so that the FIB 11 is perpendicularly radiated on the surface of the specimen 12. The FIB 11 is scanned rectangularly on the vicinity of a portion to be separated; so that a rectangular hole 13 having a required depth is formed in the surface of the specimen 12.

(b) In FIG. 3 (b) the specimen 12 is tilted so that the axis of the FIB 11 is tilted at an angle of about 70° relative to the surface of the specimen 12. The FIB 11 is radiated to a side portion of the specimen 12 in which the rectangular hole 13 is formed, so that a bottom hole 14 is formed in parallel to the surface of the portion to be separated. The tilt angle of the specimen 12 (the attitude of the specimen 12) is changed by means of 1 specimen rotator.

20 (c) In FIG. 3 (c), the attitude of the specimen 12 is changed so that the surface of the specimen 12 is set to be perpendicular to the FIB 11 again. The FIB 11 is scanned along a circumferential portion to be separated so that trenches are formed.

(d) In FIG. 3 (d), in order to separate the portion to be separated by using the FIB 11, the FIB 11 is scanned along the circumferential portion to be separated to elongate the trenches 15. Next, a separated specimen 19 is cut from the specimen 12. The cut-out separated specimen 19 is supported by the electrostatic probe 31.

(e) In FIG. 3 (e), the electrostatic probe 31 is manipulated to move the separated specimen 19 to a required place.

30 FIG. 4 (a) and FIG. 4(b) show an embodiment in which a portion of the specimen 12 is spirited in the same manner as in the above embodiment, and its separated specimen 19 is made into a thin film capable of being observed by a transmission electron microscope (TEM).

In FIG. 4 (a) a portion 19a of the separated specimen 19 is previously cut out to be thin. In FIG 4 (b) the thin portion 19a of the separated specimen 19 is further thinned to form a thin film by the FIB 11. The portion 19a of the specimen 19 is analyzed by a TEM. According to this embodiment, it is possible to remove a TEM specimen from a

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desired location on the specimen 12 easily and with accuracy, without destroying the specimen 12.

FIGS. 5 (a) and 5(b) show the removal of the separated specimen 19 by a mechanical assembly. The mechanical assembly can take the form of tweezers capable
5 of gripping the separated specimen 19.

One illustrative apparatus capable of practicing the invention as described above to achieve the mentioned steps is a commercially available focused ion beam instrument, such as model 9500 IL series marketed by Micrion Corporation. Electrostatic probes, capable of removing a cut segment of the wafer, are also commercially available.

10 The methods of the invention, therefore, allow in-line processing of a semiconductor wafer while preserving the parent wafer.

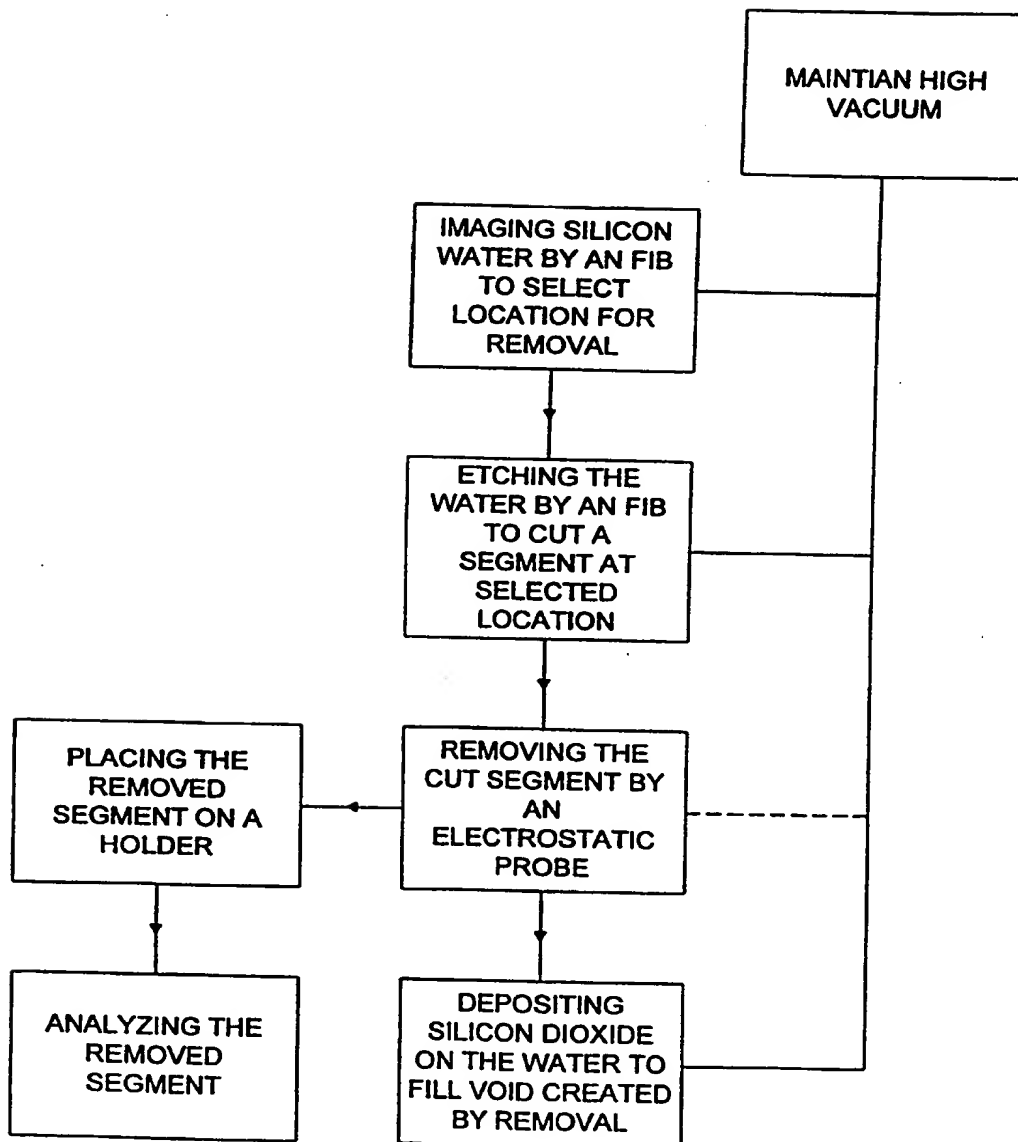
It will thus be seen that the invention attains the objectives set forth above. Because certain changes in the above processes can be made without departing from the spirit or scope of the invention, the above description is intended to be interpreted as
15 illustrative and not in a limiting sense.

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What is claimed is:

1. A method for sampling a semiconductor wafer for analysis comprising the steps
of
5 imaging said wafer, for selecting the location of a segment for sampling, by
detecting particles emitted in response to a focused ion beam incident on the wafer,
cutting said wafer at the selected location by directing a wafer-etching focused
ion beam onto the wafer to separate the segment from the wafer,
removing the separated segment from the wafer, and
10 depositing a dielectric material on the wafer surface from which said segment
was cut.
2. The method of claim 1 wherein said semiconductor wafer is silicon.
- 15 3. The method of claim 1 wherein said cut segment consists of a plurality of intact
layers, introduced by manufacturing process, with a conical shape and a cross section
selected from the group consisting of circles, ellipses, squares, and triangles.
4. The method of claim 1 wherein the step of removing said cut segment is
20 accomplished by an electrostatic probe positioned in the proximity of said cut segment.
5. The method of claim 1 wherein the step of depositing a dielectric material is
achieved by depositing silicon dioxide on the wafer surface from which said segment
was cut.
25
6. The method of claim 1 wherein the step of removing said cut segment is
accomplished by mechanical tweezers positioned in contact with said cut segment.
7. A method for sampling a semiconductor wafer for analysis comprising the steps
30 of
cutting said wafer at a selected location by directing a wafer-etching focused ion
beam onto the wafer to separate the segment from the wafer, and
removing the separated segment from the wafer using an electrostatic probe.

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**FIGURE 1**

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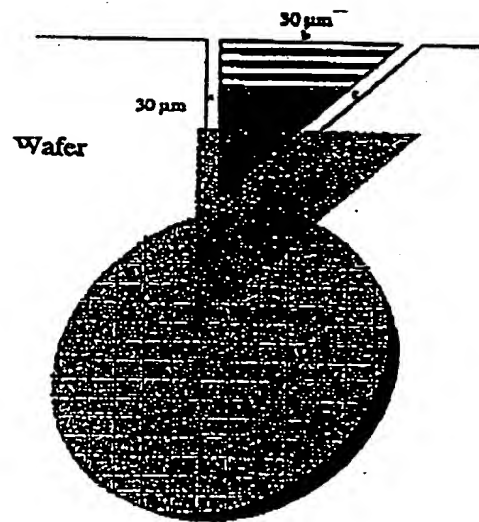


FIGURE 2

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FIG. 3a

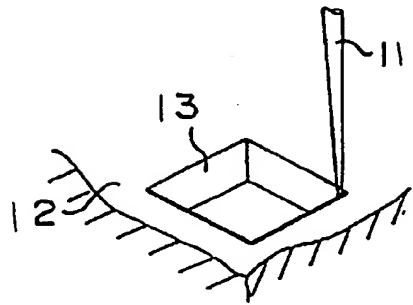


FIG. 3b

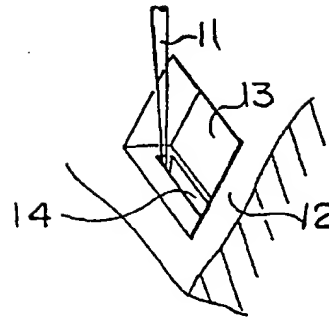


FIG. 3c

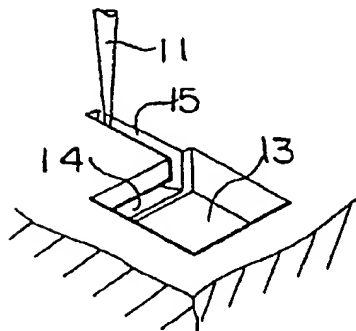


FIG. 3d

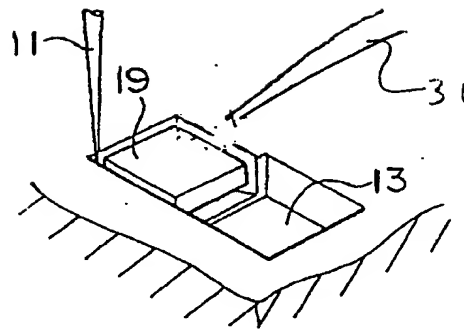
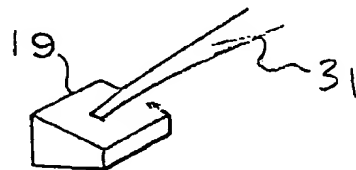


FIG. 3e



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FIG. 4a

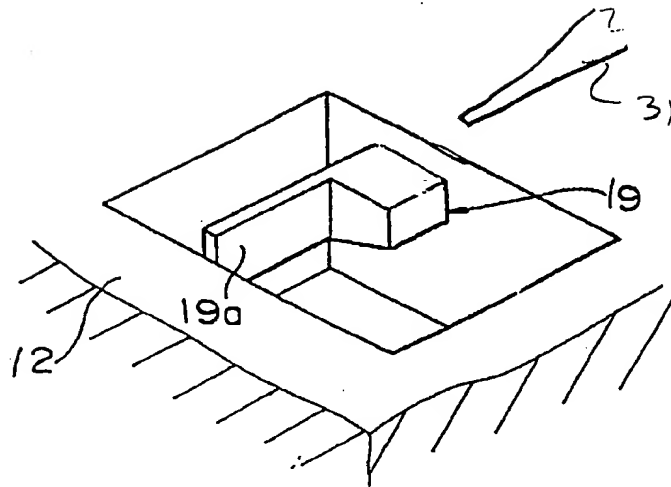


FIG. 4b

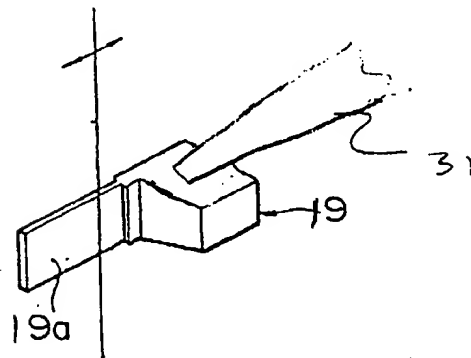


FIG. 5a

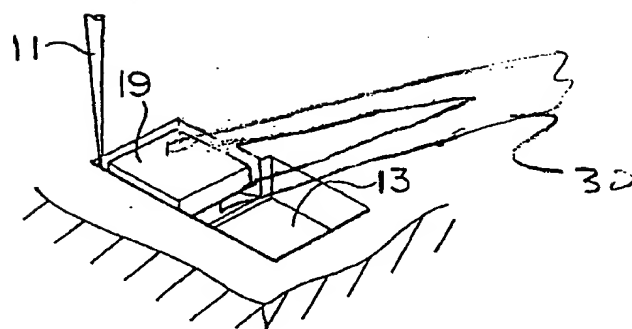
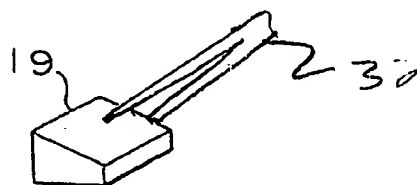


FIG. 5b



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